Please amend the claims as follows. This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-5 (cancelled)

Claim 6 (original): A semiconductor device, comprising:

a substrate having transistor devices;

a plurality of copper interconnect metallization lines and conductive vias defined in each of a plurality of interconnect levels of the semiconductor device, the plurality of copper interconnect metallization lines and conductive vias being isolated from each other by a porous dielectric material; and

a plurality of supporting stubs, each of the plurality of supporting stubs configured to form a supporting column that extends through the plurality of interconnect levels of the semiconductor device.

Claim 7 (previously amended). A semiconductor device as recited in claim 6, wherein the plurality of supporting stubs is not electrically interconnected to the plurality of copper interconnect metallization lines and conductive vias.

Claim 8 (original): A semiconductor device as recited in claim 6, further comprising:

a passivation layer defined over a topmost layer of the copper interconnect metallization lines and conductive vias.

Claims 22-25 (cancelled)

Claim 26 (previously added): A semiconductor device as recited in claim 6, wherein the plurality of copper interconnect metallization lines and conductive vias define dual damascene structures.

Claim 27 (currently amended): A semiconductor device as recited in claim 6, wherein the plurality of supporting stubs further support ~~the~~ a passivation layer.

Claim 28 (previously added): A semiconductor device, comprising:

a substrate having transistor devices; and

a plurality of copper interconnect metallization lines and conductive vias defined in each of a plurality of interconnect levels of the semiconductor device, the plurality of copper interconnect metallization lines and conductive vias being isolated from each other by a porous dielectric material.

Claim 29 (previously added): A semiconductor device as recited in claim 28, further comprising:

a plurality of supporting stubs, each of the plurality of supporting stubs configured to form a supporting column that extends through the plurality of interconnect levels of the semiconductor device.

Claim 30 (previously added): A semiconductor device as recited in claim 29, wherein the plurality of supporting stubs is not electrically interconnected to the plurality of copper interconnect metallization lines and conductive vias.

Claim 31 (previously added): A semiconductor device as recited in claim 28, further comprising:

a passivation layer defined over a topmost layer of the copper interconnect metallization lines and conductive vias.

Claim 32 (previously added): A semiconductor device as recited in claim 28, wherein the plurality of copper interconnect metallization lines and conductive vias define dual damascene structures.

Claim 33 (currently amended): A semiconductor device as recited in claim 29, wherein the plurality of supporting stubs further support ~~the~~ a passivation layer.

Claim 34 (previously added): A semiconductor device, comprising:

a substrate having transistor devices;

a plurality of copper interconnect metallization lines and conductive vias defined in each of a plurality of interconnect levels of the semiconductor device, the plurality of copper interconnect metallization lines and conductive vias being isolated from each other by a porous dielectric material; and

a passivation layer defined over a topmost layer of the copper interconnect metallization lines and conductive vias.

Claim 35 (previously added): A semiconductor device as recited in claim 34, further comprising:

a plurality of supporting stubs, each of the plurality of supporting stubs configured to form a supporting column that extends through the plurality of interconnect levels of the semiconductor device.